UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/580,223 | 05/26/2000 | Andrew Kay | YAMAP0713US | 8243 |

7590 07/12/2004

Neil A DuChez
Renner Otto Boisselle & Sklar LLP
19th Floor
1621 Euclid Avenue
Cleveland, OH 44115

| EXAMINER | |
|---|---|
| SHARON, AYAL I | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | 16 |

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/580,223 | KAY ET AL. | |
| | Examiner | Art Unit | |
| | Ayal I Sharon | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. Claims 1-13 of U.S. Application 09/580,223 filed on 05/26/2000 are presented for examination. The application claims foreign priority to U.K. Patent Application 9912232.7, dated 05/27/1999.
2. Applicants' paper #15, an amendment after RCE, filed on 04/22/2004, contains amendments to the independent claims, claims 1 and 11. New art rejections have been applied to all claims.

### *Drawings*

3. This application has been filed with informal drawings which are acceptable for examination purposes only. More specifically, the lines, numbers an letters are not uniformly thick and well defined, as required by 37 CFR 1.84(i). Formal drawings will be required when the application is allowed.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. The prior art used for these rejections is as follows:

6. Ashenden, F. et al. "Considerations on System-Level Behavioral and Structural Modeling Extensions to VHDL". Proc. 1998 Int'l Verilog HDL Conference and VHDL Int'l Users Forum. March 16-19, 1998. pp.42-50. (Henceforth referred to as "**Ashenden**").

7. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

8. **Claims 1, 4, 7-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ashenden.**

9. In regards to Claim 1, Ashenden teaches the following limitations:

1. A method of transferring data from a sender process to a plurality of receiver processes,
(Ashenden, especially: Section 5.2 "Communication Abstraction")

wherein at least one of said processes is described in a hardware description language,
(Ashenden, especially: Section 5.2 "Communication Abstraction")

In the cited section, Ashenden teaches the designing of message-passing communication in VHDL. (VHDL is a hardware description language).

said hardware description language incorporating simulation means for simulation of the behaviour of hardware and also incorporating a hardware compiler for deriving hardware which behaves according to said simulation,
(Ashenden, especially: Section 1, "Introduction")

Ashenden teaches that "A number of specialized languages may be used in designing a system. Some, such as the Unified Modeling Language, are primarily notations for expressing the relationships between the various components that make up the system. Others, including those discussed in this paper [e.g. VHDL] Once behaviour has been captured using such languages, the system can be simulated to verify that it meets its requirements. Subsequently, it can be manually or automatically refined to a more detailed implementation in terms of hardware, software, or a combination of both."

Examiner finds that it is inherent that the "... automatic refine[ment] to a more detailed implementation in terms of hardware ..." is performed by a compiler.

characterised in that the method uses a language construct which, for a given communication, defines a sender process for sending the communication and defines a plurality of receiver processes each for receiving the communication sent by the sender process, thereby effecting synchronised communication between the sender process and the receiver processes.
(Ashenden, especially: Section 5.2 "Communication Abstraction")

10. In regards to Claim 4, Ashenden teaches the following limitations:

4. A method as claimed in claim 2, characterised in that a check is made that all of the receiver processes are ready to receive data before data is transferred from the sender process to the receiver processes.
(Ashenden, especially: Section 5.2 "Communication Abstraction")

In the cited section, Ashenden teaches that "... If synchronous communication is used, the presence of multiple receivers implies a barrier beyond which none of the receivers nor the sender can pass until message transmission occurs. If asynchronous communication is used, each receiver accepts a copy of the message when it is ready. The sender proceeds as soon as it has sent the message."

Examiner there fore interprets that the claimed limitation is inherent to synchronous communication, otherwise the synchronous communication would not work correctly.

11. In regards to Claim 7, Ashenden teaches the following limitations:

7. A method as claimed in claim 1, characterised in that at least one of said processes is embodied in hardware.
(Ashenden, especially: Section 1, "Introduction")

Ashenden teaches that "A number of specialized languages may be used in designing a system. Some, such as the Unified Modeling Language, are primarily notations for expressing the relationships between the various components that make up the system. Others, including those discussed in this paper [e.g. VHDL] Once behaviour has been captured using such languages, the system can be simulated to verify that it meets its requirements. Subsequently, it can be manually or automatically refined to a more detailed implementation in terms of hardware, software, or a combination of both."

Examiner finds that it is inherent that the "... automatic refine[ment] to a more detailed implementation in terms of hardware ..." reads on the claimed limitation.

12. In regards to Claim 8, Ashenden teaches the following limitations:

8. A method as claimed in claim 1, characterised in that all of said processes are described in said hardware description language.
(Ashenden, especially: Section 5.2 "Communication Abstraction")

In the cited section, Ashenden teaches the designing of message-passing communication in VHDL. (VHDL is a hardware description language).

13. In regards to Claim 9, Ashenden teaches the following limitations:

9. A synchronous electrical circuit produced by first simulating at least part of the circuit in accordance with the method of claim 1, and then creating the circuit using said hardware compiler.
(Ashenden, especially: Section 1, "Introduction")

Ashenden teaches that "A number of specialized languages may be used in designing a system. Some, such as the Unified Modeling Language, are primarily notations for expressing the relationships between the various components that make up the system. Others, including those discussed in this paper [e.g. VHDL] Once behaviour has been captured using such languages, the system can be simulated to verify that it meets its requirements. Subsequently, it can be manually or automatically refined to a more detailed implementation in terms of hardware, software, or a combination of both."

Examiner finds that it is inherent that the "... automatic refine[ment] to a more detailed implementation in terms of hardware ..." is performed by a compiler.

14. In regards to Claim 10, Ashenden teaches the following limitations:

10. A synchronous electrical circuit as claimed in claim 9, which is a digital electronic circuit.
(Ashenden, especially: Section 1, "Introduction")

Ashenden teaches that "A number of specialized languages may be used in designing a system. Some, such as the Unified Modeling Language, are primarily notations for expressing the relationships between the various components that make up the system. Others, including those discussed in this paper [e.g. VHDL] Once behaviour has been captured using such languages, the system can be simulated to verify that it meets its requirements. Subsequently, it can be manually or automatically refined to a more detailed implementation in terms of hardware, software, or a combination of both."

Examiner finds that it is inherent that the "... automatic refine[ment] to a more detailed implementation in terms of hardware ..." reads on the claimed limitation.

15. In regards to Claim 11, Ashenden teaches the following limitations:

11. A hardware description language adapted to simulate the behaviour of at least a sender process and a plurality of receiver processes,
(Ashenden, especially: Section 5.2 "Communication Abstraction")

In the cited section, Ashenden teaches the designing of message-passing communication in VHDL. (VHDL is a hardware description language).

and comprising a language construct which, for a given communication, defines a sender process for sending the communication and defines a plurality of receiver processes each for receiving the communication sent by the sender process, thereby effecting synchronised communication between the sender process and the recciver processes.
(Ashenden, especially: Section 5.2 "Communication Abstraction")

16. In regards to Claim 12, Ashenden teaches the following limitations:

12. A hardware description language adapted to carry out the method of claim 1.
(Ashenden, especially: Section 5.2 "Communication Abstraction")

In the cited section, Ashenden teaches the designing of message-passing communication in VHDL. (VHDL is a hardware description language).

***Claim Rejections - 35 USC § 103***

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The prior art used for these rejections is as follows:

19. Ashenden, F. et al. "Considerations on System-Level Behavioral and Structural Modeling Extensions to VHDL". Proc. 1998 Int'l Verilog HDL Conference and VHDL Int'l Users Forum. March 16-19, 1998. pp.42-50. (Henceforth referred to as "**Ashenden**").

20. Hoare, C.A.R. "Communicating Sequential Processes". Communications of the ACM. Vol.21, Issue 8. August 1978. pp.666-677. (Henceforth referred to as "**Hoare**").

21. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

**22. Claims 2-3 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ashenden in view of Hoare.**

23. In regards to Claim 2, Ashenden does not expressly teach the following limitations:

2. A method as claimed in claim 1 which involves carrying out a send algorithm under the control of a pre-emptive scheduler.

Hoare, on the other hand, does expressly teach this limitation. See the first 3 paragraphs of Section 5, "Monitors and Scheduling", in particular:

> ... Any attempted output from X(j) will be delayed until a subsequent iteration, after the output of some other process X(i) has been accepted and dealt with.
>
> Similarly, conditions can be used to delay acceptance of inputs which would violate scheduling constraints – postponing them until some later occasion when some other process has brought the monitor into a state in which the input can validly be accepted.

Examiner interprets that the delay mechanism corresponds to the claimed "pre-emptive scheduler".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ashenden with those of Hoare, because Ashenden expressly teaches (Seep.46, left column) that "Synchronous message passing, on the other hand, is more amenable to formal analysis, and properties such as freedom from deadlock and livelock can be expressed using CSP" (CSP is the Hoare reference, "Communicating Sequential Processes").

24. In regards to Claim 3, Ashenden does not expressly teach the following limitations:

3. A method as claimed in claim 2, characterised in that the scheduler ensures that the send algorithm is carried out without descheduling.

Hoare, on the other hand, does expressly teach this limitation. See the first 3 paragraphs of Section 5, "Monitors and Scheduling", in particular:

> ... Any attempted output from X(j) will be delayed until a subsequent iteration, after the output of some other process X(i) has been accepted and dealt with.
>
> Similarly, conditions can be used to delay acceptance of inputs which would violate scheduling constraints – postponing them until some later occasion when some other process has brought the monitor into a state in which the input can validly be accepted.

Examiner interprets that the delay mechanism corresponds to the claimed "pre-emptive scheduler".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ashenden with those of Hoare, because Ashenden expressly teaches (Seep.46, left column) that "Synchronous message passing, on the other hand, is more amenable to formal analysis, and properties such as freedom from deadlock and livelock can be expressed using CSP" (CSP is the Hoare reference, "Communicating Sequential Processes").

25. In regards to Claim 5, Ashenden does not expressly teach the following limitations:

5. A method as claimed in claim 1 which involves carrying out a receive algorithm under the control of a pre-emptive scheduler.

Hoare, on the other hand, does expressly teach this limitation. See the first 3 paragraphs of Section 5, "Monitors and Scheduling", in particular:

> ... Any attempted output from X(j) will be delayed until a subsequent iteration, after the output of some other process X(i) has been accepted and dealt with.
>
> Similarly, conditions can be used to delay acceptance of inputs which would violate scheduling constraints – postponing them until some later occasion when some other process has brought the monitor into a state in which the input can validly be accepted.

Examiner interprets that the delay mechanism corresponds to the claimed "pre-emptive scheduler".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ashenden with those of Hoare, because Ashenden expressly teaches (Seep.46, left column) that "Synchronous message passing, on the other hand, is more amenable to formal analysis, and properties such as freedom from deadlock and livelock can be expressed using CSP" (CSP is the Hoare reference, "Communicating Sequential Processes").

26. In regards to Claim 6, Ashenden does not expressly teach the following limitations:

> 6. A method as claimed in claim 5, characterised in that the scheduler ensures that the receive algorithm is carried out without descheduling.

Hoare, on the other hand, does expressly teach this limitation. See the first 3 paragraphs of Section 5, "Monitors and Scheduling", in particular:

> ... Any attempted output from X(j) will be delayed until a subsequent iteration, after the output of some other process X(i) has been accepted and dealt with.
>
> Similarly, conditions can be used to delay acceptance of inputs which would violate scheduling constraints – postponing them until some later occasion when some other process has brought the monitor into a state in which the input can validly be accepted.

Examiner interprets that the delay mechanism corresponds to the claimed "pre-emptive scheduler".

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Ashenden with those of Hoare, because Ashenden expressly teaches (Seep.46, left column) that "Synchronous message passing, on the other hand, is more amenable to formal analysis, and properties such as freedom from deadlock and livelock can be expressed using CSP" (CSP is the Hoare reference, "Communicating Sequential Processes").

27. **Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ashenden in view of Official Notice.**

28. In regards to Claim 13, Ashenden does not expressly teach the following limitations:

13. A computer readable medium carrying a computer program adapted to carry out the method of claim 1.

Official Notice is given that it was well known at the time the invention was made to store computer programs on computer

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ashenden's teachings regarding VHDL and VHDL compilers with those of Official Notice, because doing so would create a permanent record of the computer software, and would eliminate the need to retype the entire computer program each type it was run.

***Response to Arguments***

*Re: Drawings*

29. Examiner acknowledges Applicants statement (paper #9, p.2) that they will provide formal drawings if the application is allowed.

*Re: Double Patenting*

30. In paper #15, p.5, Applicants persuasively argue that the amended version of Claim 1 of the present application is not an obvious variation of Claim 1 in U.S. Patent 6,201,266 ("**Kay '266**"). Examiner has therefore withdrawn the double patenting rejections of Claims 1-10.

*Re: Claim Rejections - 35 USC § 102*

31. In paper #15, pp.6-10, Applicants persuasively argue that the amended version of Claims 1 and 11 of the present application are not taught or anticipated by U.K. Patent 2,317,245 ("**Kay '245**"). Examiner has therefore withdrawn the all rejections based on the Kay '245 reference.

***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is

(703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
2121 Crystal Drive
Arlington, VA

The fax phone number is: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

June 30, 2004